	L #	Hits	Search Text	DBs
1	L1	141	((((instruction prefetch$3 fetch$3) near5 (queue buffer)) near20 cache) near20 (line block)) near99 branch	USPAT; US-PGPUB
2	L3	12	((instruction prefetch$3 fetch$3) near5 (queue buffer)) near99 (branch near20 (short bound$3 cross$3 across) near20 (line bound$3 block))	USPAT; US-PGPUB
3	L7	320	((instruction prefetch$3 fetch$3) near5 (queue buffer)) near99 (branch near20 (short wrap$4 bound$3 cross$3 across line block)) not 3	USPAT; US-PGPUB
4	L8	195	((instruction prefetch$3 fetch$3) near5 (queue buffer)) near99 (branch near20 (short wrap$4 bound$3 cross$3 across line block)) not (1 3)	USPAT; US-PGPUB
5	L6	42	((instruction prefetch$3 fetch$3) near5 (queue buffer)) near99 (branch near20 (short wrap$4 bound$3 cross$3 across)) not 3	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040 00321 7 A1	☐	Data processing device with branch prediction mechanism	712/239
2	US 20030 22600 3 A1	☐	Information processor having delayed branch function	712/238
3	US 61192 20 A	☐	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
4	US 60353 87 A	☐	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
5	US 59960 71 A	☐	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
6	US 59481 00 A	☐	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
7	US 59037 51 A	☐	Method and apparatus for implementing a branch target buffer in CISC processor	712/238
8	US 58058 76 A	☐	Method and system for reducing average branch resolution time and effective misprediction penalty in a processor	712/234
9	US 57348 81 A	☐	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
10	US 57064 92 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/238
11	US 57014 48 A	☐	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
12	US 51426 34 A	☐	Branch prediction	712/240

	Document ID	U	Title	Current OR
1	US 20040 00320 2 A1	☐	Instruction fetch control apparatus	712/205
2	US 20010 05205 3 A1	☒	Stream processing unit for a multi-streaming processor	711/138
3	US 64426 81 B1	☒	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
4	US 64271 90 B1	☒	Configurable cache allowing cache-type and buffer-type access	711/129
5	US 63413 24 B1	☒	Exception processing in superscalar microprocessor	710/260
6	US 62567 15 B1	☒	System and method of performing gateway access	711/163
7	US 61758 97 B1	☒	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
8	US 61015 90 A	☒	Virtual memory system with local and global virtual address translation	711/203
9	US 60527 76 A	☒	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
10	US 59789 09 A	☒	System for speculative branch target prediction having a dynamic prediction history buffer and a static prediction history buffer	712/240
11	US 59516 79 A	☒	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
12	US 59260 53 A	☒	Selectable clock generation mode	327/298
13	US 58389 61 A	☒	Method of operation and apparatus for optimizing execution of short instruction branches	712/233
14	US 58260 70 A	☒	Apparatus and method for maintaining status flags and condition codes using a renaming technique in an out of order floating point execution unit	712/222
15	US 58190 60 A	☒	Instruction swapping in dual pipeline microprocessor	712/219
16	US 58156 93 A	☒	Processor having a frequency modulated core clock based on the criticality of program activity	713/501
17	US 58156 92 A	☒	Distributed clock generator	713/501
18	US 57649 39 A	☒	RISC processor having coprocessor for executing circular mask instruction	712/205
19	US 57427 80 A	☒	Dual pipeline superscalar reduced instruction set computer system architecture	712/206
20	US 57404 10 A	☒	Static clock generator	713/501
21	US 57375 62 A	☒	CPU pipeline having queuing stage to facilitate branch instructions	712/218
22	US 57179 46 A	☒	Data processor	712/225

	Document ID	U	Title	Current OR
23	US 5644744 A	☒	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
24	US 5640526 A	☒	Superscaler instruction pipeline having boundary indentification logic for variable length instructions	712/207
25	US 5625787 A	☒	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
26	US 5603047 A	☒	Superscalar microprocessor architecture	712/23
27	US 5295248 A	☒	Branch control circuit	712/239
28	US 5167026 A	☒	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
29	US 5148528 A	☒	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
30	US 5142633 A	☒	Preprocessing implied specifiers in a pipelined processor	712/225
31	US 4258429 A	☒	Multiphase clocking for MOS electronic calculator or digital processor chip	712/32
32	US 4037090 A	☒	Multiphase clocking for MOS	708/130
33	US 4024386 A	☒	Electronic calculator or digital processor chip having test mode of operation	714/718
34	US 4021781 A	☒	Virtual ground read-only-memory for electronic calculator or digital processor	711/211
35	US 4021656 A	☒	Data input for electronic calculator or digital processor chip	708/139
36	US 4012600 A	☒	Automatic pushbutton dial system for a subscriber telephone	379/357.04
37	US 4011414 A	☒	Automatic dial system for a subscriber telephone	379/357.05
38	US 3991306 A	☒	Electronic calculator or digital processor chip with separately controllable digit and segment outputs	708/168
39	US 3991305 A	☒	Electronic calculator or digital processor chip with multiple code combinations of display and keyboard scan outputs	708/168
40	US 3989939 A	☒	Electronic calculator or digital processor chip with combined functions for constant, keyboard and control bit	708/190
41	US 3988604 A	☒	Electronic calculator or digital processor chip having multiple function arithmetic unit output	708/190
42	US 3764988 A	☐	INSTRUCTION PROCESSING DEVICE USING ADVANCED CONTROL SYSTEM	712/234

	Document ID	U	Title	Current OR
1	US 20040 01568 3 A1	☐	Two dimensional branch history table prefetching mechanism	712/240
2	US 20030 13571 9 A1	☒	Method and system using hardware assistance for tracing instruction disposition information	712/227
3	US 20030 13571 8 A1	☒	Method and system using hardware assistance for instruction tracing by revealing executed opcode or instruction	712/227
4	US 20030 02875 8 A1	☒	SINGLE ARRAY BANKED BRANCH TARGET BUFFER	712/238
5	US 20020 19913 7 A1	☒	Microcontroller with debug support unit	714/30
6	US 20020 12082 9 A1	☒	Data processer and data processing system	712/207
7	US 20020 09991 0 A1	☒	High speed low power cacheless computer system	711/117
8	US 20010 04746 7 A1	☒	METHOD AND APPARATUS FOR BRANCH PREDICTION USING FIRST AND SECOND LEVEL BRANCH PREDICTION TABLES	712/228
9	US 20010 03230 9 A1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
10	US 20010 01873 5 A1	☒	Data processor and data processing system	712/207
11	US 66717 81 B1	☒	Data cache store buffer	711/138
12	US 66623 14 B1	☒	Microcomputer including program for rewriting data in an internal flash memory	714/42
13	US 65976 64 B1	☒	Digital circuit synthesis system	370/252
14	US 65713 31 B2	☒	Static branch prediction mechanism for conditional branch instructions	712/239
15	US 65534 88 B2	☒	Method and apparatus for branch prediction using first and second level branch prediction tables	712/239
16	US 65429 82 B2	☒	Data processer and data processing system	712/207
17	US 65021 88 B1	☒	Dynamic classification of conditional branches in global history branch prediction	712/234
18	US 64991 01 B1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
19	US 64346 91 B1	☒	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205

	Document ID	U	Title	Current OR
20	US 6418525 B1	☒	Method and apparatus for reducing latency in set-associative caches using set prediction	711/213
21	US 6405303 B1	☒	Massively parallel decoding and execution of variable-length instructions	712/210
22	US 6339822 B1	☒	Using padded instructions in a block-oriented cache	712/213
23	US 6307488 B1	☒	LZW data compression and decompression apparatus and method using grouped data characters to reduce dictionary accesses	341/51
24	US 6292884 B1	☒	Reorder buffer employing last in line indication	712/216
25	US 6272624 B1	☒	Method and apparatus for predicting multiple conditional branches	712/239
26	US 6256728 B1	☒	Processor configured to selectively cancel instructions from its pipeline responsive to a predicted-taken short forward branch instruction	712/236
27	US 6253287 B1	☒	Using three-dimensional storage to make variable-length instructions appear uniform in two dimensions	711/125
28	US 6250821 B1	☒	Method and apparatus for processing branch instructions in an instruction buffer	712/238
29	US 6249862 B1	☒	Dependency table for reducing dependency checking hardware	712/218
30	US 6247120 B1	☒	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
31	US 6240524 B1	☒	Semiconductor integrated circuit	713/500
32	US 6240508 B1	☒	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
33	US 6237074 B1	☒	Tagged prefetch and instruction decoder for variable length instruction set and method of operation	711/213
34	US 6233676 B1	☒	Apparatus and method for fast forward branch	712/233
35	US 6209084 B1	☒	Dependency table for reducing dependency checking hardware	712/233
36	US 6185675 B1	☒	Basic block oriented trace cache utilizing a basic block sequence buffer to indicate program order of cached basic blocks	712/238
37	US 6175909 B1	☒	Forwarding instruction byte blocks to parallel scanning units using instruction cache associated table storing scan block boundary information for faster alignment	712/204
38	US 6167510 A	☒	Instruction cache configured to provide instructions to a microprocessor having a clock cycle time less than a cache access time of said instruction cache	712/239
39	US 6154833 A	☒	System for recovering from a concurrent branch target buffer read with a write allocation by invalidating and then reinstating the instruction pointer	712/238
40	US 6108769 A	☒	Dependency table for reducing dependency checking hardware	712/216
41	US 6101577 A	☒	Pipelined instruction cache and branch prediction mechanism therefor	711/125
42	US 6067610 A	☒	Method and data processor for synchronizing multiple masters using multi-bit synchronization indicators	712/21

	Document ID	U	Title	Current OR
43	US 6052708 A	☒	Performance monitoring of thread switch events in a multithreaded processor	718/108
44	US 6044459 A	☒	Branch prediction apparatus having branch target buffer for effectively processing branch instruction	712/237
45	US 6044450 A	☒	Processor for VLIW instruction	712/24
46	US 6032251 A	☒	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
47	US 6026477 A	☒	Branch recovery mechanism to reduce processor front end stall time by providing path information for both correct and incorrect instructions mixed in the instruction pool	712/2
48	US 5983335 A	☒	Computer system having organization for multiple condition code setting and for testing instruction out-of-order	712/23
49	US 5978908 A	☒	Computer instruction supply	712/240
50	US 5974535 A	☒	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
51	US 5963725 A	☒	Simulation system and method for microcomputer program	703/17
52	US 5960467 A	☒	Apparatus for efficiently providing memory operands for instructions	711/214
53	US 5956495 A	☒	Method and system for processing branch instructions during emulation in a data processing system	703/26
54	US 5931944 A	☒	Branch instruction handling in a self-timed marking system	712/239
55	US 5920710 A	☒	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
56	US 5918045 A	☒	Data processor and data processing system	712/237
57	US 5897654 A	☒	Method and system for efficiently fetching from cache during a cache fill operation	711/131
58	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
59	US 5881308 A	☒	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions out-of-order	712/23
60	US 5881260 A	☒	Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction	712/210
61	US 5873115 A	☒	Cache memory	711/129
62	US 5870612 A	☒	Method and apparatus for condensed history buffer	710/260
63	US 5870579 A	☒	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
64	US 5870575 A	☒	Indirect unconditional branches in data processing system emulation mode	712/209
65	US 5867698 A	☒	Apparatus and method for accessing a branch target buffer	712/238

	Document ID	U	Title	Current OR
66	US 5864697 A	☒	Microprocessor using combined actual and speculative branch history prediction	712/240
67	US 5860014 A	☒	Method and apparatus for improved recovery of processor state using history buffer	710/260
68	US 5845100 A	☒	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
69	US 5835968 A	☒	Apparatus for providing memory and register operands concurrently to functional units	711/214
70	US 5832259 A	☒	Apparatus for superscalar instruction pre-decoding using cached instruction lengths	712/238
71	US 5822576 A	☒	Branch history table with branch pattern field	712/239
72	US 5822575 A	☒	Branch prediction storage for storing branch prediction information such that a corresponding tag may be routed with the branch instruction	712/239
73	US 5812838 A	☒	Branch history table	712/239
74	US 5809320 A	☒	High-performance multi-processor having floating point unit	712/34
75	US 5809294 A	☒	Parallel processing unit which processes branch instructions without decreased performance when a branch is taken	712/233
76	US 5805853 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
77	US 5794027 A	☒	Method and apparatus for managing the execution of instructons with proximate successive branches in a cache-based data processing system	712/238
78	US 5787266 A	☒	Apparatus and method for accessing special registers without serialization	712/216
79	US 5784604 A	☒	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
80	US 5768555 A	☒	Reorder buffer employing last in buffer and last in line bits	712/216
81	US 5752259 A	☒	Instruction cache configured to provide instructions to a microprocessor having a clock cycle time less than a cache access time of said instruction cache	711/125
82	US 5752014 A	☒	Automatic selection of branch prediction methodology for subsequent branch instruction based on outcome of previous branch prediction	712/240
83	US 5732235 A	☒	Method and system for minimizing the number of cycles required to execute semantic routines	712/209
84	US 5692167 A	☒	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
85	US 5649145 A	☒	Data processor processing a jump instruction	711/213
86	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
87	US 5634119 A	☒	Computer processing unit employing a separate millicode branch history table	712/240
88	US 5634047 A	☒	Method for executing branch instructions by processing loop end conditions in a second processor	712/241

	Document ID	U	Title	Current OR
89	US 5632023 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
90	US 5630157 A	☒	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions	712/23
91	US 5625785 A	☒	Information processing apparatus having dual buffers for transmitting debug data to an external debug unit	712/227
92	US 5617550 A	☒	Data processor generating jump target address of a jump instruction in parallel with decoding of the instruction	712/207
93	US 5608885 A	☒	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
94	US 5606676 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/239
95	US 5542058 A	☒	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
96	US 5515521 A	☒	Circuit and method for reducing delays associated with contention interference between code fetches and operand accesses of a microprocessor	711/3
97	US 5513330 A	☒	Apparatus for superscalar instruction predecoding using cached instruction lengths	712/204
98	US 5511175 A	☒	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
99	US 5488730 A	☒	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
100	US 5481689 A	☒	Conversion of internal processor register commands to I/O space addresses	711/202
101	US 5473764 A	☒	Multilevel instruction cache	712/207
102	US 5471591 A	☒	Combined write-operand queue and read-after-write dependency scoreboard	712/217
103	US 5463748 A	☒	Instruction buffer for aligning instruction sets using boundary detection	712/204
104	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
105	US 5442766 A	☒	Method and system for distributed instruction address translation in a multiscalar data processing system	711/204
106	US 5442756 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
107	US 5418917 A	☒	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
108	US 5394529 A	☒	Branch prediction unit for high-performance processor	712/240
109	US 5386519 A	☒	Information processing apparatus incorporating buffer storing a plurality of branch target instructions for branch instructions and interrupt requests	712/238
110	US 5333296 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171
111	US 5317720 A	☒	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143

	Document ID	U	Title	Current OR
112	US 5317701 A	☒	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
113	US 5287467 A	☒	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
114	US 5265213 A	☒	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
115	US 5226130 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
116	US 5197136 A	☒	Processing system for branch instruction	712/238
117	US 5175827 A	☒	Branch history table write control system to prevent looping branch instructions from writing more than once into a branch history table	712/240
118	US 5155843 A	☒	Error transition mode for multi-processor system	714/5
119	US 5127091 A	☒	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
120	US 5113370 A	☒	Instruction buffer control system using buffer partitions and selective instruction replacement for processing large instruction loops	712/241
121	US 4994919 A	☒	Pipeline microcomputer having branch instruction detector and bus controller for producing and carrying branch destination address prior to instruction execution	712/233
122	US 4937784 A	☒	Data processor with efficient transfer between subroutines and main program	712/228
123	US 4954947 A	☒	Instruction processor for processing branch instruction at high speed	712/218
124	US 4884244 A	☒	Method of addressing a computer memory	365/240
125	US 4882701 A	☒	Lookahead program loop controller with register and memory for storing number of loop times for branch on count instructions	712/241
126	US 4858105 A	☒	Pipelined data processor capable of decoding and executing plural instructions in parallel	712/235
127	US 4761731 A	☒	Look-ahead instruction fetch control for a cache memory	711/156
128	US 4742453 A	☒	Pipeline-controlled information processing system for generating updated condition code	712/234
129	US 4742451 A	☒	Instruction prefetch system for conditional branch instruction for central processor unit	712/235
130	US 4725947 A	☒	Data processor with a branch target instruction storage	712/238
131	US 4691277 A	☒	Small instruction cache using branch target table to effect instruction prefetch	711/213
132	US 4679141 A	☒	Pageable branch history table	712/240
133	US 4604691 A	☒	Data processing system having branch instruction prefetching performance	712/207

	Document ID	U	Title	Current OR
134	US 4477872 A	☒	Decode history table for conditional branch instructions	712/240
135	US 4212077 A	☒	Text processing system for displaying and editing a line of text	715/530
136	US 4200927 A	☒	Multi-instruction stream branch processing mechanism	712/235
137	US 4179736 A	☒	Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit	712/232
138	US 4161026 A	☒	Hardware controlled transfers to microprogram control apparatus and return via microinstruction restart codes	712/232
139	US 4156906 A	☒	Buffer store including control apparatus which facilitates the concurrent processing of a plurality of commands	711/128
140	US 4156279 A	☒	Microprogrammed data processing unit including a multifunction secondary control store	712/209
141	US 4156278 A	☒	Multiple control store microprogrammable control unit including multiple function register control field	712/248
142	US 4048624 A	☒	Calculator system having multi-function memory instruction register	712/32
143	US 3986010 A	☒	Automatic tool deflection calibration system	700/195
144	US 3940741 A	☒	Information processing device for processing instructions including branch instructions	712/238
145	US 3924110 A	☒	Calculator system featuring a subroutine register	708/130
146	US 3922538 A	☒	Calculator system featuring relative program memory	708/190
147	US 3919536 A	☒	Precharged digital adder and carry circuit	708/684
148	US 3919532 A	☒	Calculator system having an exchange data memory register	708/190
149	US 3916169 A	☒	Calculator system having a precharged virtual ground memory	365/203
150	US 3904863 A	☒	Calculator system using instruction words as data	708/190
151	US 3904862 A	☒	Calculator system having a constant memory	708/190
152	US 3902054 A	☒	Calculator system having keyboard with double entry protection and serialized encoding	708/139
153	US 3900722 A	☒	Multi-chip calculator system having cycle and subcycle timing generators	708/190
154	US 3614747 A	☒	INSTRUCTION BUFFER SYSTEM	711/125
155	US 3577189 A	☐	APPARATUS AND METHOD IN A DIGITAL COMPUTER FOR ALLOWING IMPROVED PROGRAM BRANCHING WITH BRANCH ANTICIPATION REDUCTION OF THE NUMBER OF BRANCHES, AND REDUCTION OF BRANCH DELAYS	712/219